

REMARKS/ARGUMENTS

The Office Action has been carefully considered. Reconsideration and allowance in view of the foregoing amendments and the following remarks is respectfully requested.

Claims 1–4 were rejected under 35 U.S.C. § 112 and 35 U.S.C. § 103. Claims 1-4 are canceled without prejudice. New claims 5-17 are added.

Double Patenting Rejection

Examiner provisionally rejected claim 1 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of copending Application No. 10/506,234. Applicant respectfully traverses this rejection. Applicant has canceled claims 1-4 and added new claims 5-17. The newly added claims 5-17 are patentably distinct from the claims of copending Application No. 10/506,234. Applicant respectfully requests that the Examiner withdraw the provisional double patenting rejection.

Claim Rejections - 35 USC § 112

Examiner rejected claims 1-4 under 35 USC § 112, second paragraph, as being indefinite. Applicant has canceled claims 1-4 without prejudice and has added new claims 5-17. New claims 5-17 particularly point out and distinctly claim the subject matter which applicant regards as the invention, thus satisfying 35 USC § 112, second paragraph.

Applicant notes that the newly added independent claims, claim 5 and claim 13, are broader than canceled claim 1. Thus, the new claims 5-17 are entitled to their full scope of doctrine of equivalents.

Claim Rejections - 35 USC § 103

Examiner rejected claims 1 and 3-4 under 35 USC § 103 as being unpatentable over U.S. Patent No. 6,370,664 (hereinafter “Bhawmik”) in view of the official notice taken by the Examiner. Examiner rejected claim 2 under 35 USC § 103 as being

unpatentable over Bhawmik (6,370,664) in view of U.S. Patent No. 5,574,733 (hereinafter “Kim”). Applicant has canceled claims 1-4, thus making these rejections moot. However, since new claims 5-17 are broader in scope than canceled claims 1-4, a discussion of Bhawmik and Kim with respect to new claims 5-17 is provided below to expedite the prosecution of this application.

Claim 5 recites (emphasis added):

5. An integrated circuit comprising;

a test circuit that generates deterministic test vectors;

an application circuit coupled to receive and process the deterministic test vectors to produce output signals;

a logic gate coupled to receive the output signals and block X signal portions of the output signals in response to a first signal and output the remainder of the output signals; and

a signature register coupled to receive the remainder of the output signals and generate a signature.

Bhawmik discloses a system for testing an integrated circuit using a scan chain, made up of a plurality of flip flops. Bhawmik teaches that the plurality of flip flops may be used as a single scan chain or selectively partitioned into smaller scan chains which can be “simultaneously latched and provided test results.” Column 3, lines 9-20. “The scan chain is switchable between a partitioned and a non-partitioned configuration, so that either configuration can be selected on demand, thereby allowing both BIST and deterministic testing to be performed efficiently on the same circuit.” Column 3, lines 15-19.

Bhawmik does not disclose or teach “a logic gate coupled to receive the output signals and block X signal portions of the output signals in response to a first signal and output the remainder of the output signals.” The XOR gates discussed in Bhawmik and

illustrated in figures 2 and 3 are for partitioning a scan chain of flip flops into smaller scan chains. See Column 4, line 66 – Column 5, line 6. There is no disclosure, suggestion or teaching in Bhawmik for blocking “X signal portions of the output signals in response to a first signal and output the remainder of the output signals.” Nor would it have been obvious to one skilled in the art to modify Bhamik to include this missing limitation.

Further, the Kim reference does not disclose, teach or suggest this limitation of claim 5. Kim discloses a scan chain that includes a linear feedback shift register (LFSR) cascaded with a shift register to “simultaneously generate test patterns and compress test results during a built-in self test (BIST) sequence.” Column 3, lines 60-67. Again, Kim fails to disclose, teach or suggest “a logic gate coupled to receive the output signals and block X signal portions of the output signals in response to a first signal and output the remainder of the output signals.” Nor would it have been obvious to one skilled in the art to modify Kim to include this missing limitation.

Claims 6-12 depend from claim 5 and are allowable for the same reasons discussed above with respect to claim 5. In addition, independent claim 13 includes similar limitations to those found in claim 5 and is also believed by Applicant to be in condition for allowance. Claims 14-17 depend from claim 13 and are also believed by the Applicant to be in condition for allowance.

Conclusion

Applicant believes that sufficient reasons have been stated to traverse all of the rejections. Accordingly, additional reasons are not presented in order to avoid unnecessary and/or cumulative arguments. However, Applicant reserves the right to challenge any assertions made the Examiner in the Office Action that are not herein addressed. Furthermore, it should be noted that the absence of any discussion specific to those rejections is in no way an acceptance by acquiescence by the Applicant.

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Atty. Docket No. : DE02 0018 US
Amendment Date : December 16, 2005

In view of the above arguments and amendments, Applicant believes that all pending claims are allowable and respectfully request a Notice of Allowance for this application. Should the Examiner believe that a telephone conference would expedite the prosecution of this application, the undersigned can be reached at (650) 856-7539.

If any fees are due in connection with the filing of this amendment, the Commissioner is authorized to charge such fees to Deposit Account 50-2776.

Date: Dec. 16, 2005

Respectfully submitted,

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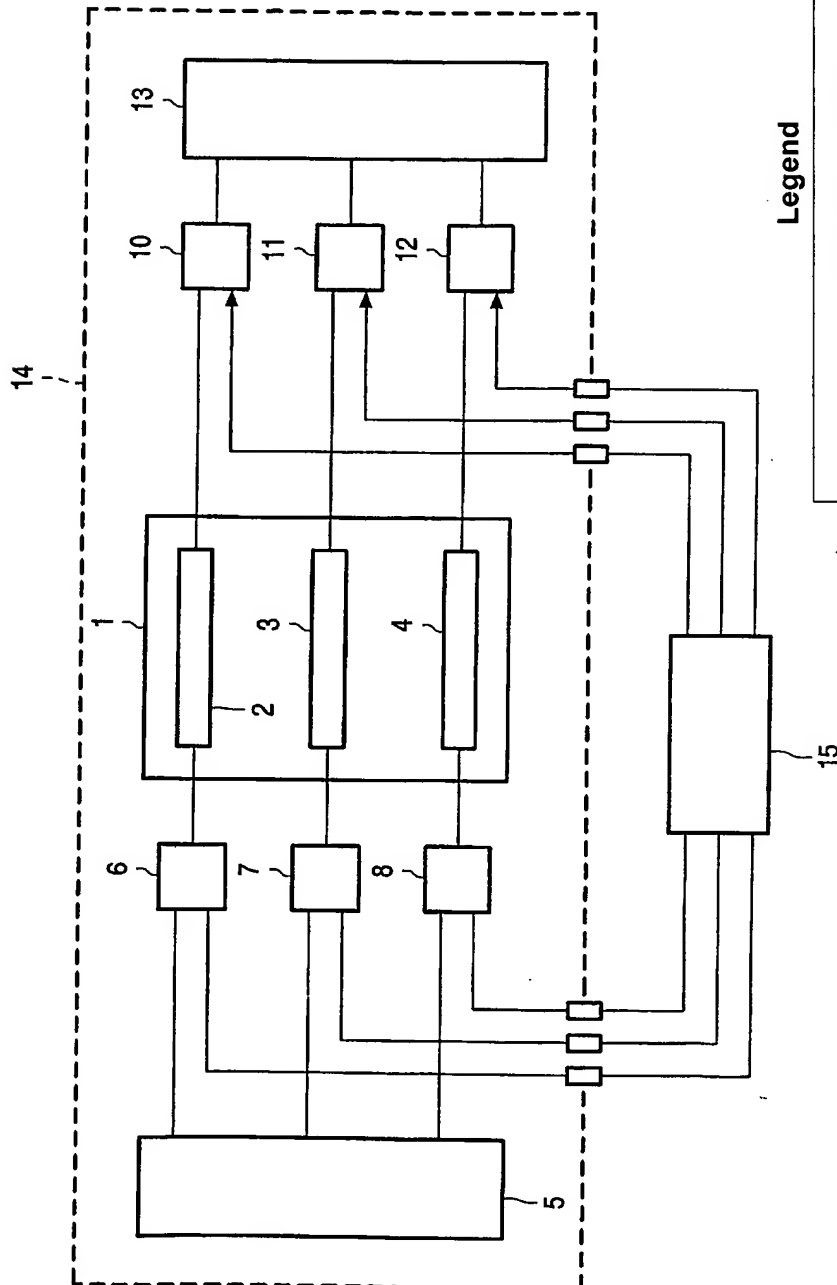
Amendments to the Drawings:

Examiner objected to the drawings under 37 C.F.R 1.84(o), stating that “[a]ll features represented by boxes in the drawing must be label with a term which indicates what element the boxes represent.” The original drawing includes reference numbers that correspond to written description in the specification. Applicant submits herewith a replacement sheet for the original drawing that includes a legend matching the reference numbers to the corresponding term used in the specification. No new matter is being introduced.

Attachment: Replacement Sheet
Annotated Sheet Showing Changes



1/1



Legend

Application Circuit
Shift Registers
Linear Feedback Shift Register
First Logic Gates
Second Logic Gates
Signature Register
Integrated Circuit
Test Setup

1
2, 3, 4
5
6, 7, 8
10, 11, 12
13
14
15

Legend
Added